Introduction to Computer Architecture

COE 308 – Computer Architecture

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What is "Computer Architecture" ?

- ❖ Computer Architecture =

  Instruction Set Architecture +
  Computer Organization

- ❖ Instruction Set Architecture (ISA)
  - ✸ WHAT the computer does (logical view)
- ❖ Computer Organization
  - ✸ HOW the ISA is implemented (physical view)
- ❖ We will study both in this course

Why Study Computer Architecture?

- ❖ You want to be called “Computer Engineer or Scientist”
- ❖ You want to become an “expert” on computer hardware
- ❖ You want to become a “computer system designer”
- ❖ You want to become a “software designer” and need to understand how to improve code performance
- ❖ Technology is improving rapidly ⇒ new opportunities
- ❖ Has never been more exciting!
- ❖ Impacts Electrical Engineering and Computer Science

Which Books will be Used?

- ❖ Computer Organization & Design
  The Hardware/Software Interface
  - ✷ David Patterson and John Hennessy
  - ✷ Morgan Kaufmann Publishers
  - ✷ Third Edition (2005) is available in bookstore
  - ✷ Read the textbook in addition to the course slides



- ❖ References: MIPS32 Architecture
  - ✷ Volumes I, II, and III are available online



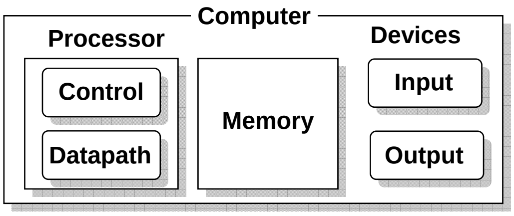
- ❖ Course webpage
  - ✷ http://www.ccse.kfupm.edu.sa/~mudawar/coe308/

Course Objectives

- ❖ Understand modern computers, their evolution, and trade-offs at the HW/SW interface
  - ✸ Instruction Set Architecture
  - ✸ Computer Arithmetic
  - ✸ Performance and Metrics
  - ✸ Pipelining
- ❖ Understand the design of a modern computer system
  - ✸ Datapath design
  - ✸ Control design
  - ✸ Memory System Design
  - ✸ I/O System Design

Five Classic Components

- ❖ Since the 1940's, computers have 5 classic components



- ❖ Input devices
  - ✸ Keyboard, mouse, …
- ❖ Output devices
  - ✸ Display, printer, …
- ❖ Storage devices
  - ✸ Volatile memory devices: DRAM, SRAM, …
  - ✸ Permanent storage devices: Magnetic, Optical, and Flash disks, …
- ❖ Datapath
- ❖ Control

} **Together, they are called the Processor**

- ❖ Newly added 6th component: Network
  - ✸ Essential component for communication in any computer system

Fetch - Execute Cycle

Infinite Cycle implemented in Hardware

Instruction Fetch	**Obtain instruction from program storage**
Instruction Decode	**Determine required actions and instruction size**
Operand Fetch	**Locate and obtain operand data**
Execute	**Compute result value and status**
Writeback Result	**Deposit results in storage for later use**
Next Instruction	**Determine successor instruction**

Instruction Set Architecture (ISA)

- ❖ Is a subset of Computer Architecture
- ❖ Definition by Amdahl, Blaaw, and Brooks – 1964

  "… the attributes of a [computing] system as seen by the programmer, i.e. the conceptual structure and functional behavior, as distinct from the organization of the data flows and controls the logic design, and the physical implementation."

- ❖ An ISA encompasses …
  - ✸ Instructions and Instruction Formats
  - ✸ Data Types, Encodings, and Representations
  - ✸ Programmable Storage: Registers and Memory
  - ✸ Addressing Modes: Accessing Instructions and Data
  - ✸ Handling Exceptional Conditions

Instruction Set Architecture – cont'd

- Critical interface between hardware and software
  - Standardizes instructions, machine language bit patterns, etc.
  - Advantage: different implementations of the same architecture
  - Disadvantage: sometimes prevents using new innovations

- Examples

Examples	(versions)	Introduced in
Intel	(8086, 80386, Pentium, ...)	1978
IBM Power	(Power 2, 3, 4, 5)	1985
HP PA-RISC	(v1.1, v2.0)	1986
MIPS	(MIPS I, II, III, IV, V)	1986
Sun Sparc	(v8, v9)	1987
Digital Alpha	(v1, v3)	1992
PowerPC	(601, 604, …)	1993

Overview of the MIPS ISA

- All instructions are 32-bit wide
- Instruction Categories
  - Load/Store
  - Integer Arithmetic
  - Jump and Branch
  - Floating Point
  - Memory Management
- Three Instruction Formats

Registers

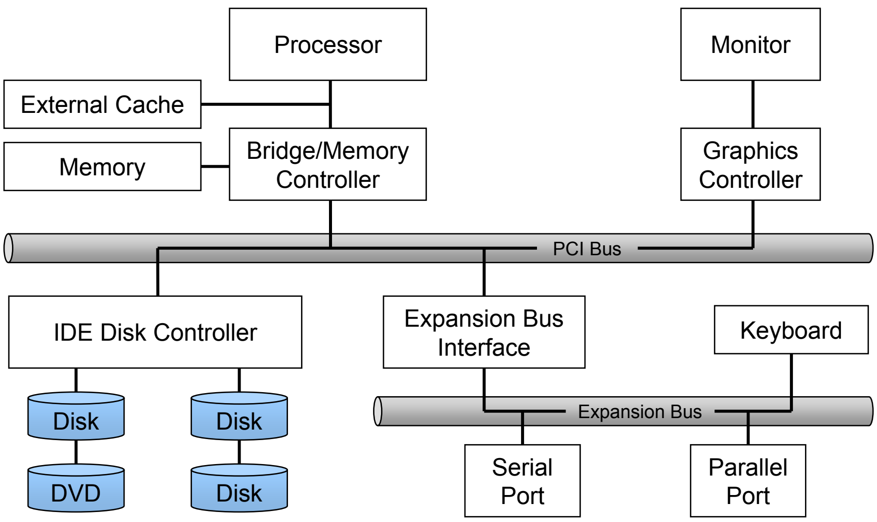
Registers
R0 - R31
PC
HI
LO

R-type	Op^6	Rs^5	Rt^5	Rd^5	sa^5	$funct^6$
I-type	Op^6	Rs^5	Rt^5	$immediate^{16}$		
J-type	Op^6	$immediate^{26}$				

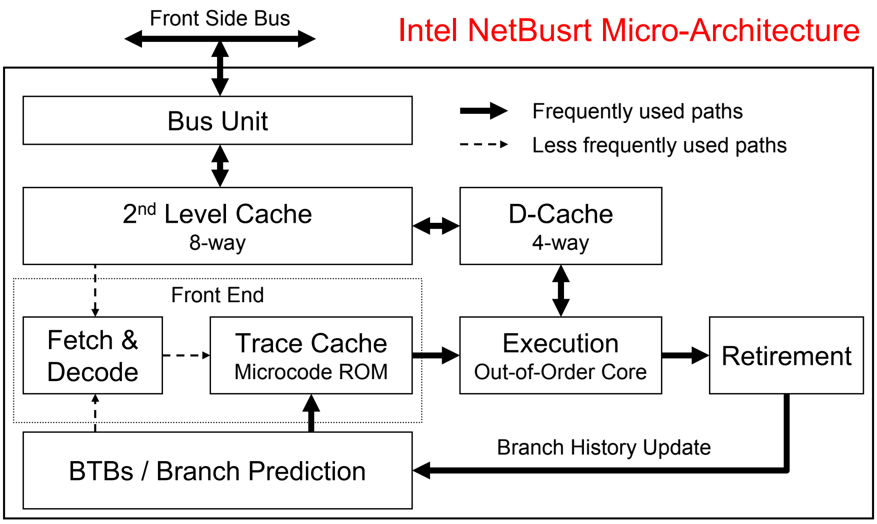
Computer Organization

- Realization of the Instruction Set Architecture
- Characteristics of principal components
  - Registers, ALUs, FPUs, Caches, ...
- Ways in which these components are interconnected
- Information flow between components
- Means by which such information flow is controlled
- Register Transfer Level (RTL) description

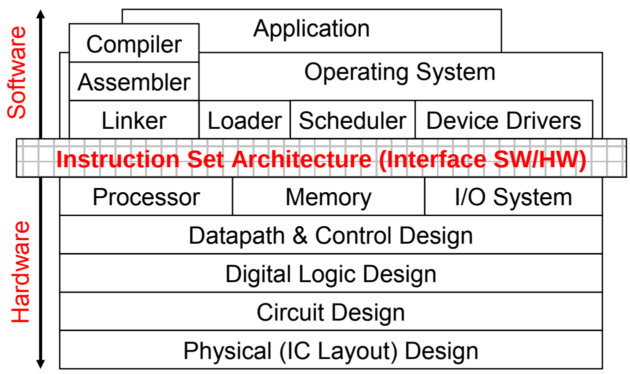
Desktop Computer Organization



Microprocessor Organization



Abstraction Layers



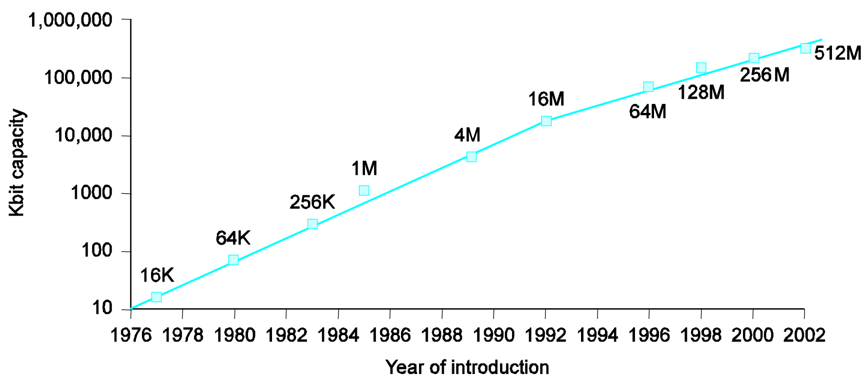
- Abstraction hides implementation details between levels
- Helps us cope with enormous complexity
- ISA is at the interface between software and hardware

Technology Improvements

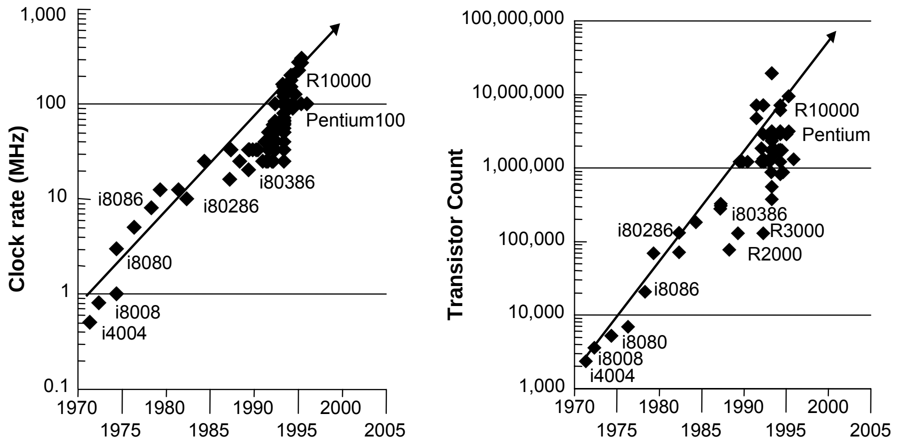
- ❖ Vacuum tube → transistor → IC → VLSI
- ❖ Processor
  - ✸ Transistor count: about 30% to 40% per year
  - ✸ Clock rate: about 20% to 30% per year
- ❖ Memory
  - ✸ DRAM capacity: about 60% per year (4x every 3 yrs)
  - ✸ Memory speed: about 10% per year
  - ✸ Cost per bit: decreases about 25% per year
- ❖ Disk
  - ✸ Capacity: about 60% per year
- ❖ Opportunities for new applications
- ❖ Better organizations and designs

Growth of Capacity per DRAM Chip

- ❖ DRAM capacity quadrupled almost every 3 years
  - ✸ 60% increase per year, for 20 years



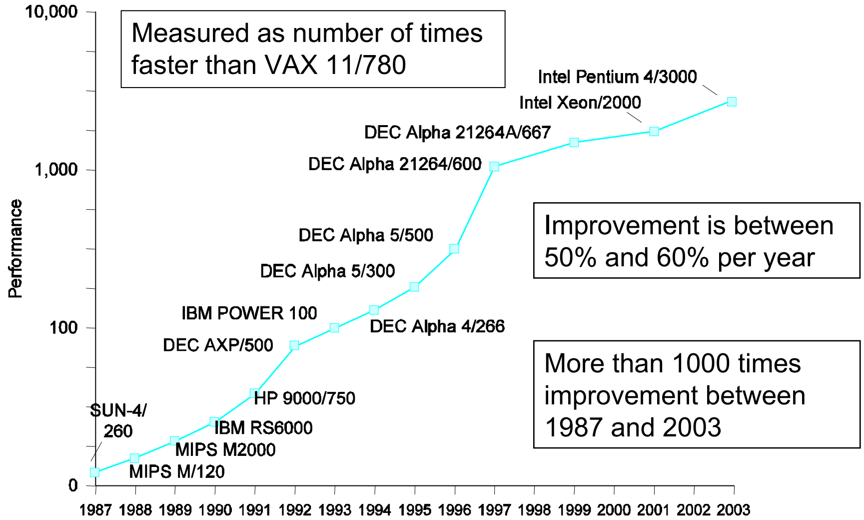
Clock Rate and Transistor Count



20% to 30% per year

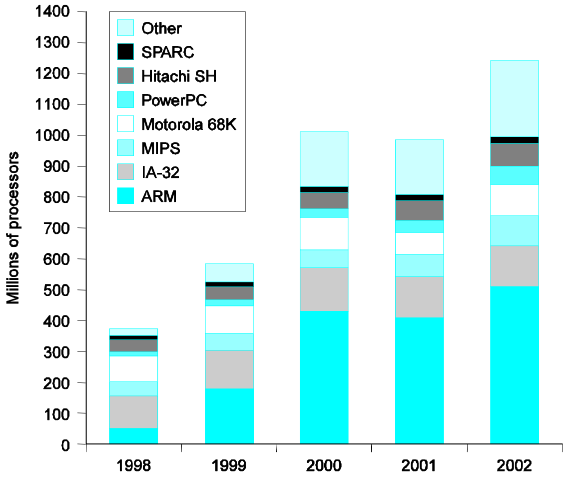
30% to 40% per year

Workstation Performance

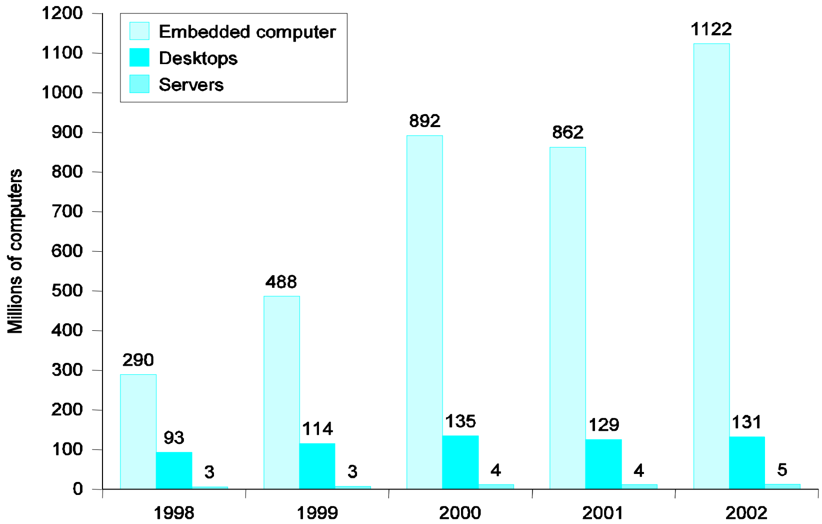


Microprocessor Sales (1998 - 2002)

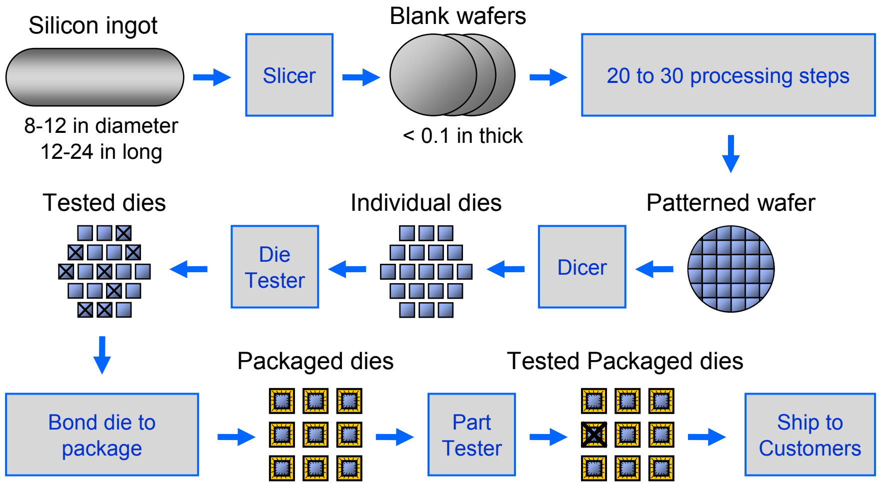
- ARM processor sales exceeded Intel IA-32 processors, which came second
- ARM processors are used mostly in cellular phones
- Most processors today are embedded in cell phones, video games, digital TVs, PDAs, and a variety of consumer devices



Microprocessor Sales - cont'd

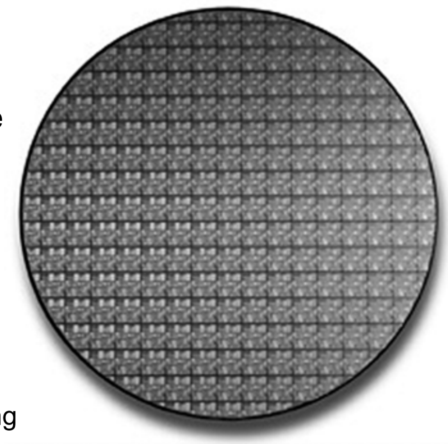


Chip Manufacturing Process

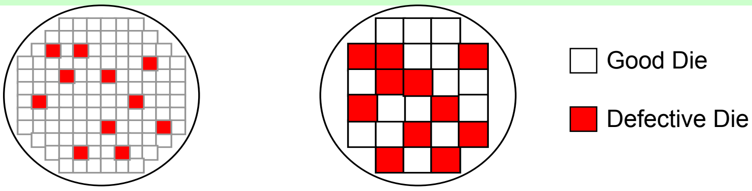


Wafer of Pentium 4 Processors

- 8 inches (20 cm) in diameter
- Die area is 250 mm^2
  - About 16 mm per side
- 55 million transistors per die
  - 0.18 μm technology
  - Size of smallest transistor
  - Improved technology uses
    - 0.13 μm and 0.09 μm
- Dies per wafer = 169
  - When yield = 100%
  - Number is reduced after testing
  - Rounded dies at boundary are useless



Effect of Die Size on Yield



120 dies, 109 good

26 dies, 15 good

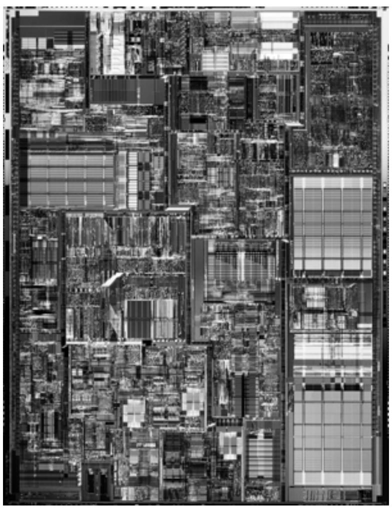
Dramatic decrease in yield with larger dies

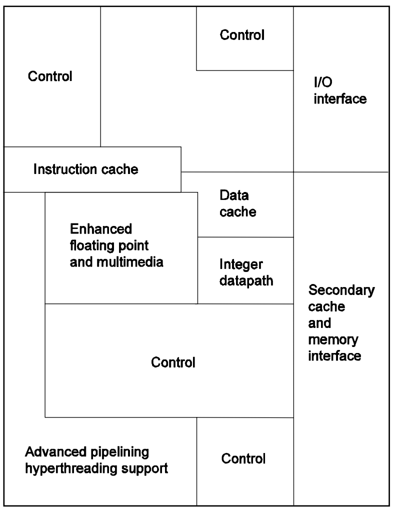
Yield = (Number of Good Dies) / (Total Number of Dies)

$$\text{Yield} = \frac{1}{(1 + (\text{Defect per area} \times \text{Die area} / 2))^2}$$

Die Cost = (Wafer Cost) / (Dies per Wafer × Yield)

Inside the Pentium 4 Processor Chip





Intel x86 Processor Evolution

Processor	Year	Clock	Transistors	Registers	Data Bus	Max Memory	Caches
8086	1978	8 MHz	29 K	GP: 16 bits	16 bits	1 MB	None
80286	1982	12 MHz	134 K	GP: 16 bits	16 bits	16 MB	None
80386	1985	20 MHz	275 K	GP: 32 bits	32 bits	4 GB	None
80486	1989	25 MHz	1.2 M	GP: 32 bits FP: 80 bits	32 bits	4 GB	L1: 8KB
Pentium	1993	60 MHz	3.1 M	GP: 32 bits FP: 80 bits	64 bits	4 GB	L1:16K
Pentium Pro	1995	200 MHz	5.5 M	GP: 32 bits FP: 80 bits	64 bits	64 GB	L1:16K L2:256K
Pentium II	1997	266 MHz	7 M	GP: 32 bits FP: 80 bits MMX: 64b	64 bits	64 GB	L1:32K L2:256K
Pentium III	1999	500 MHz	8.2 M	GP: 32 bits FP: 80 bits MMX: 64b XMM: 128b	64 bits	64 GB	L1:32K L2:512K

Intel x86 Processor Evolution – cont'd

Processor	Year	Clock	Transistors	Registers	MicroArch	Bandwidth	Caches
Pentium 4	2000	1.5 GHz	42 M	GP: 32 bits FP: 80 bits MMX: 64b XMM: 128b	NetBurst	3.2 GB/s	Trace:12Kop L1:8K L2:256K
Pentium 4 with Hyper-Threading	2002	2.2 GHz	55 M	GP: 32 bits FP: 80 bits MMX: 64b XMM: 128b	NetBurst Hyper-Threading	3.2 GB/s	Trace:12Kop L1:8K L2:512K

Course Roadmap

- ❖ Instruction set architecture (Chapter 2)
- ❖ Computer arithmetic (Chapter 3)
- ❖ Performance issues (Chapter 4)
- ❖ Constructing a processor (Chapter 5)
- ❖ Pipelining to improve performance (Chapter 6)
- ❖ Memory: caches and virtual memory (Chapter 7)
- ❖ Disk Storage and Input/Output (Chapter 8)

Key to obtain a good grade: read the textbook!